SAMPLE

Building the Microcontrollers of Tomorrow

A Practical Guide to the Embedded Systems Reshaping Hardware

Aiman JoeHanz

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Contents

Introduction

Chapter 1: Current Microcontroller Landscape

Chapter 2: Limitations and Challenges

Chapter 3: Solutions and Innovations

Chapter 4: Feature Deep-Dives

Chapter 5: Outdated Technologies and Future Outlook

Chapter 6: Conclusion and Recommendations

Chapter 7: Advanced Microcontroller Architectures

Chapter 8: Internet of Things and Connected Microcontrollers

Chapter 9: Embedded AI and TinyML

Chapter 10: Real-Time Operating Systems for Microcontrollers

Chapter 11: Power Management for Battery-Operated Devices

Chapter 12: Microcontroller Development Tools and Workflow

Chapter 13: Interfacing with Sensors and Actuators

Chapter 14: Communication Protocols Deep Dive

Chapter 15: PCB Design Considerations for Microcontroller Projects

Chapter 16: Microcontroller Selection Guide

Chapter 17: Testing and Quality Assurance for Embedded Systems

Chapter 18: Manufacturing and Production

Chapter 19: Career Paths in Embedded Systems

Chapter 20: Motor Control with Microcontrollers

Chapter 21: Wireless Communication Implementation

Chapter 22: Memory Management in Embedded Systems

Chapter 23: Display and User Interface Implementation

Chapter 24: Microcontroller Security Best Practices

Chapter 25: The Future of Microcontrollers

Chapter 26: Real-Time Operating Systems Deep Dive

Chapter 27: Power Optimization Techniques

Chapter 28: Testing and Debugging Strategies

Chapter 29: ADC and DAC Implementation

Chapter 30: Communication Protocol Implementation Details

Chapter 31: Microcontroller Selection Guide

Chapter 32: Sensor Integration

Chapter 33: PCB Design Considerations for Microcontroller Projects

Chapter 34: Manufacturing and Scaling

Chapter 35: Interrupt Handling Deep Dive

Chapter 36: Bootloader Design and OTA Updates

Chapter 37: TinyML — Machine Learning on Microcontrollers

Chapter 38: Summary and the Path Forward

Chapter 39: FPGA vs Microcontroller — When to Use What

This free sample contains the Introduction and Chapter 1. The complete book contains the full contents above.

Introduction

Microcontrollers are the invisible workhorses of the modern world. They are in your phone, your car, your refrigerator, your toothbrush, and increasingly in devices that didn't have electronics a decade ago. In 2026, 40 billion microcontrollers ship annually — six for every person on Earth. They are the silicon substrate of the Internet of Things, the brains behind smart homes and smart cities, and the foundation upon which the AI edge revolution is being built.

This book examines the current state of microcontroller technology — from 8-bit relics to 32-bit powerhouses with AI acceleration — and projects where the field is heading through 2036. It covers ten key domains: architecture evolution, RISC-V disruption, AI at the edge, security, low-power design, connectivity, development tools, real-time systems, IoT applications, and the future of embedded silicon.

The research draws on technical specifications from ARM, RISC-V International, Espressif, STMicroelectronics, and other silicon vendors, combined with hands-on experience with development boards and real-world embedded projects. Predictions are grounded in semiconductor roadmaps and the physical limits of silicon scaling.

This book is part of the Building of Tomorrow series. Each volume provides technical depth without losing accessibility, and strategic context without losing rigor.

This research draws on the work of the ARM, RISC-V, and open-source embedded communities. Any errors or omissions are solely the responsibility of the author.

-- Aiman JoeHanz August 2026

Chapter 1: Current Microcontroller Landscape

- IEEE Spectrum: The Rise of RISC-V (2025) - ARM: Cortex-M Processor Family White Paper (2026) - RISC-V International: Annual Report 2025 - Yole Group: MCU Industry Report 2026 - ## 2.1 ARM Cortex-M Ecosystem

The ARM Cortex-M family remains the dominant force in 32-bit microcontrollers. The 2026 lineup includes:

The 2026 Cortex-M lineup spans the full spectrum of capability:

- Cortex-M0+ (ARMv6-M, 2-stage pipeline): no FPU, DSP, or vector support; up to 50 MHz. Typical use: ultra-low-power designs. - Cortex-M3 (ARMv7-M, 3-stage pipeline): no FPU; DSP instructions; up to 150 MHz. Typical use: general purpose. - Cortex-M4 (ARMv7E-M, 3-stage pipeline): FPU and DSP; up to 240 MHz. Typical use: DSP and motor control. - Cortex-M7 (ARMv7E-M, 6-stage pipeline): FPU and DSP; up to 600 MHz. Typical use: high performance. - Cortex-M23 (ARMv8-M, 2-stage pipeline): TrustZone security; up to 80 MHz. Typical use: security-focused designs. - Cortex-M33 (ARMv8-M, 3-stage pipeline): FPU, DSP, and TrustZone; up to 150 MHz.

Typical use: security plus DSP. - Cortex-M55 (ARMv8.1-M, 6-stage pipeline): FPU, DSP, and Helium vector extension; up to 400 MHz. Typical use: edge AI. - Cortex-M85 (ARMv8.1-M, 6-stage pipeline): FPU, DSP, and vector support; up to 550 MHz. The highest-performance Cortex-M. Introduced with ARMv8.1-M, Helium provides M-Profile Vector Extension (MVE) for: - 128-bit vector processing (4x 32-bit or 8x 16-bit operations per cycle) - Integer and floating-point vector operations - 4x DSP performance improvement over Cortex-M4F - 15x ML performance improvement for quantized models - Zero-overhead loop instructions

ARMv8-M introduces TrustZone for hardware-isolated secure/non-secure execution: - Two execution states: Secure and Non-secure - Hardware-enforced memory partitioning (SAU, MPU) - Secure boot chain from immutable ROM - Secure element emulation (replacing external SE chips)

KEY TAKEAWAYS - The ARM Cortex-M family remains the dominant force in 32-bit microcontrollers.

RISC-V has emerged as the primary alternative to ARM in the MCU space:

The commercial RISC-V MCU landscape in 2026 spans everything from ten-cent parts to application-class chips:

- SiFive E76 (RV32GC, 500 MHz, 4 MB external flash, 1.6 MB RAM): FPU and

MMU — the performance end of the spectrum. - WCH CH32V003 (RV32EC, 48 MHz, 16 KB flash, 2 KB RAM): the ten-cent MCU, for cost-driven designs. - Espressif ESP32-C6 (RV32IMAC, 160 MHz, 512 KB flash, 320 KB RAM): Wi-Fi 6 and BLE 5 in a RISC-V package. - GigaDevice GD32VF1 (RV32IMAC, 108 MHz, 128 KB flash, 32 KB RAM): pin-compatible with STM32 parts, easing migration. - Nuclei N300 (RV32IMAFC, 320 MHz, 256 KB flash, 128 KB RAM): RISC-V with DSP extensions. - Bouffalo BL808 (RV64GC, 480 MHz, 16 MB flash, 192 KB RAM): an AI accelerator on a 64-bit RISC-V core. - M: Integer multiplication/division - A: Atomic operations (multi-core support) - C: Compressed instructions (16-bit encoding for code density) - F/D: Single/double-precision floating point - V: Vector operations (variable-length vectors) - B: Bit manipulation - K: Cryptography (AES, SHA, SM-ciphers) - Zce: Custom embedded extension (zero-extend, bit manipulation)

The leading Wi-Fi plus BLE combo chips in 2026:

- ESP32-S3 (Espressif, Xtensa LX7): Wi-Fi 4 and BLE 5.0, 512 KB flash and 512 KB RAM, vector instructions for AI workloads. - ESP32-C6 (Espressif, RISC-V): Wi-Fi 6 and BLE 5.3, 512 KB flash and 320 KB RAM, the low-power option. - nRF5340 (Nordic, Cortex-M33): BLE 5.1 only, 512 KB flash and 128 KB RAM, dual-core architecture with a network processor. - EFR32MG24 (Silicon Labs, Cortex-M33): BLE Mesh, 1.5 MB flash and 256 KB RAM, built for secure Zigbee/Thread designs. - CYW55572 (Infineon, Cortex-M4): Wi-Fi 6 and BLE 5.4, 2 MB flash and 1 MB RAM, with Thread support. Cellular IoT MCUs integrate the modem and the application processor:

- nRF9161 (Nordic): LTE-M/NB-IoT on 3GPP Release 17, with a Cortex-M33 application core — a single-chip cellular device. - BG770A (Quectel): LTE Cat 1 modem that pairs with an external MCU, for designs that want to keep the modem and application domains separate. - EXS82 (Thales): LTE-M/NB modem with an integrated Cortex-M4 application core.

The TinyML movement has enabled ML inference on microcontrollers with less than 1MB of RAM: - TensorFlow Lite for Microcontrollers: Runs 20KB models on Cortex-M0+ - NNoM (NNoM Neural Network on Microcontroller): C-based inference engine - Edge Impulse: Cloud platform generating optimized MCU models - CMSIS-NN: ARM-optimized neural network kernels

MCUs with dedicated AI hardware bring neural acceleration to embedded power budgets:

- STM32N6 (Cortex-M55 core, NPU at 0.6 TOPS, 4 MB RAM): vision and audio inference on-device. - MAX78002 (Cortex-M4 core, CNN accelerator at 0.5 TOPS, 1 MB RAM): keyword spotting. - K210 (Kendryte, RV64GC, KPU at 0.5

TOPS, 8 MB RAM): low-cost vision. - ESP32-S3 (Xtensa LX7, vector instructions at roughly 0.1 TOPS, 512 KB RAM): audio workloads.

- Apollo4 Plus (Cortex-M4F, NPU at 0.2 TOPS, 1 MB RAM): health and wearable sensing.

- Flash: 16KB to 4MB, 10,000-100,000 write cycles - SRAM: 2KB to 1MB, volatile - EEPROM: 256B to 4KB, 1M write cycles - External: QSPI flash (up to 16MB), PSRAM (up to 8MB)

- MRAM (Magnetoresistive RAM): Non-volatile, 100T+ write cycles, 200ns access. Used in STM32L5, RP2040. - FRAM (Ferroelectric RAM): Non- volatile, 10T+ write cycles. Used in TI MSP430FR. - OTPA (One-Time Programmable

Area): Factory calibration and secure boot keys. - TCAM

(Ternary CAM): Hardware lookup tables for fast rule matching. - Cache: Instruction and data caches on Cortex-M7/M85 (up to 64KB combined).

- Raspberry Pi RP2040: 8 PIO state machines, 32 instructions each, independently clocked - Custom protocols: Implement any serial protocol (VGA, DPI, I2S, SPI variants) without hardware support - Dedicated DMA: Each PIO state machine has dedicated DMA channels for autonomous data transfer

- Motor control timers: 16-bit with complementary PWM, dead-time insertion, fault detection - High-resolution timers: 184 ps resolution on STM32HRTIM for switch-mode power supplies - Frequency counter: Direct hardware frequency measurement with gate time control

- Hardware crypto engines: AES-128/256, SHA-1/256, HMAC, RSA-2048/4096, ECC P-256/P-384 - True Random Number Generators: NIST SP 800-90A compliant, entropy from thermal noise - Secure debug: Debug access controlled by secure boot — can be permanently locked - Active tamper detection: Temperature, voltage, and physical tamper sensors

- STM32CubeIDE: Eclipse-based, free, STM32-specific - PlatformIO: Multi-platform, 1,200+ boards, library manager - Arduino IDE 2.0: Simplified, huge community, supports many ARM and RISC-V boards - VS Code + CMake: Modern, with Cortex-Debug and RISC-V extensions - Zephyr SDK: RTOS- aware, multi-architecture

- SWD/JTAG: Standard debug interfaces on all modern MCUs - Trace (ITM/ ETM): Real-time instruction and data trace - Energy profiling: Otii Arc, Joulescope for current profiling down to nA resolution - Logic analyzers: Saleae, Sigrok for protocol decoding

The 2026 microcontroller landscape is characterized by: - ARM Cortex-M

dominance challenged by RISC-V adoption - Edge AI moving from cloud to MCU (TinyML) - Wireless integration (Wi-Fi 6, BLE 5.4, cellular IoT) - Security built-in from the start (TrustZone, secure boot) - Memory innovations (MRAM, FRAM for non-volatile operation) - Rich peripheral sets including programmable I/O - Mature development ecosystems

- ARM: Cortex-M55 and M85 Technical Reference Manual - RISC-V International: ISA Specifications - STMicroelectronics: STM32N6 Datasheet - Espressif: ESP32-C6 Reference Manual - TinyML Foundation: State of TinyML 2026 Report - Nordic Semiconductor: nRF9161 Product Brief - Yole Group: MCU Market Report 2026 - SiFive: E76 Family Product Page

End of free sample. The full book is available at putrabooks.github.io

ABOUT THE AUTHOR

Aiman JoeHanz writes about the technologies that are quietly reshaping the world. His Building of Tomorrow series examines the infrastructure behind artificial intelligence -- from blockchain and cloud computing to agentic systems and token optimization -- and asks how these technologies will evolve over the coming decade.

His books are built on technical research and engineering documentation, written for readers who want to understand systems rather than trends. He covers what is being built today and what it will take to build what comes next.

He believes that understanding infrastructure is the difference between watching the future happen and helping to create it.